In the Claims:

1. (Currently Amended) A method of planarizing a semiconductor wafer, the method comprising:

a) filling gaps between metal interconnect lines formed on a wafer by depositing HDP fill on top of the metal interconnects and between the metal interconnects to create an HDP overfill;

b) contacting the surface of the HDP overfill with a fixed abrasive polishing pad; and

c) relatively moving said wafer and said fixed abrasive polishing pad to affect a polishing rate sufficient to reach a predetermined endpoint and a substantially planar surface on the wafer sufficiently close above the metal interconnect lines and yet far enough away from said lines to prevent damage to said ~~lines~~ lines, said predetermined endpoint on the wafer being equal to or less than about 50nm.

2. (Original) The method of claim 1 wherein said metal interconnect lines are selected from the group consisting of aluminum, titanium, copper, tungsten and mixtures thereof.

3. (Original) The method of claim 2 wherein said metal interconnect lines are aluminum.

4. (Original) The method of claim 2 wherein said metal interconnect lines are titanium.

5. (Original) The method of claim 2 wherein said metal interconnect lines are copper.

6. (Original) The method of claim 2 wherein said metal interconnect lines are tungsten.

7-15. Cancelled.

16. (Currently Amended) In a method of planarizing a semiconductor wafer, the improvement comprising polishing above metal interconnect lines to uniformly polish the topography of the wafer to a predetermined endpoint on the wafer sufficiently close above the metal interconnect lines, yet far enough away from said lines to prevent damage to the lines, comprising:

a) filling gaps between metal interconnect lines of an inter metal dielectric in a wafer being formed, by depositing HDP fill on top of the metal interconnects, between the metal interconnects, and on the surface of a dielectric layer between said metal interconnects to create an HDP overfill;

b) contacting the surface of HDP overfill of the processed semiconductor wafer from step a) with a fixed abrasive polishing pad; and

c) relatively moving said wafer and said fixed abrasive polishing pad to affect a polishing rate sufficient to reach a predetermined endpoint and uniformly planar surface on the wafer sufficiently close above the metal interconnect lines and yet far enough away from said lines to prevent damage to said ~~lines~~ lines, said predetermined endpoint on the wafer being equal to or less than about 50nm.